WHAT IS CLAIMED IS:

1. An integrated circuit, comprising:

a transistor level comprising one or more semiconductor devices disposed over a substrate and an overlying transistor isolation layer having one or more contact vias extending therethrough;

a ferroelectric device level comprising one or more ferroelectric capacitors disposed over the transistor isolation layer and an overlying ferroelectric isolation layer having one or more vias extending therethrough and laterally sized larger than corresponding contact vias aligned therewith;

a first metal level disposed over the ferroelectric device level;

an inter-level dielectric level disposed over the first metal level; and

a second metal level disposed over the inter-level dielectric level.

2. The subject matter of claim 1, wherein the contact vias are filled with tungsten contact plugs.

3. The subject matter of claim 2, wherein the ferroelectric capacitors are formed over respective tungsten contact plugs.

4. An integrated circuit, comprising:

a transistor level comprising one or more semiconductor devices disposed over a substrate and an overlying transistor isolation layer having one or more contact vias extending therethrough;

an integrated first metal and ferroelectric device level comprising one or more first metal contacts and one or more ferroelectric capacitors disposed over the transistor isolation layer and a ferroelectric isolation layer having one or more vias extending therethrough;

an inter-level dielectric level disposed over the integrated first metal and ferroelectric device level; and

a second metal level disposed over the inter-level dielectric level.

5. The subject matter of claim 4, wherein the contact vias are filled with tungsten contact plugs.

6. The subject matter of claim 5, wherein the ferroelectric capacitors are formed over respective tungsten contact plugs.

7. The subject matter of claim 4, wherein the integrated first metal and ferroelectric device level has a thickness corresponding substantially to the ferroelectric capacitor heights.

8. The subject matter of claim 4, wherein the integrated first metal and ferroelectric device level is substantially non-planar with a reduced thickness in non-capacitor regions.

9. An integrated circuit, comprising:

a transistor level comprising one or more semiconductor devices disposed over a substrate and an overlying transistor isolation layer having one or more contact vias extending therethrough;

a first metal level disposed over the transistor isolation layer;

a ferroelectric device level comprising one or more ferroelectric capacitors disposed over the first metal level and an overlying ferroelectric isolation layer having one or more vias extending therethrough;

an inter-level dielectric level disposed over the ferroelectric device level; and

a second metal level disposed over the inter-level dielectric level.

10. The subject matter of claim 9, wherein the contact vias are filled with tungsten contact plugs.

11. The subject matter of claim 10, wherein the ferroelectric capacitors are formed over respective tungsten contact plugs.

12. An integrated circuit, comprising:

a transistor level comprising one or more semiconductor devices disposed over a substrate and an overlying transistor isolation layer having one or more contact vias extending therethrough;

a first metal level disposed over the transistor isolation layer;

an inter-level dielectric level disposed over the first metal level;

a ferroelectric device level comprising one or more ferroelectric capacitors disposed over the inter-level dielectric level and an overlying ferroelectric isolation layer having one or more vias extending therethrough; and

a second metal level disposed over the ferroelectric isolation layer.

13. The subject matter of claim 12, wherein the contact vias are filled with tungsten contact plugs.

14. The subject matter of claim 13, wherein the ferroelectric capacitors are formed over respective tungsten contact plugs.

15. An integrated circuit, comprising:

a transistor level comprising one or more semiconductor devices disposed over a substrate and an overlying transistor isolation layer;

a ferroelectric device level comprising one or more ferroelectric capacitors disposed over the transistor isolation layer and an overlying ferroelectric isolation layer having one or more vias extending through the ferroelectric isolation layer and the transistor isolation layer;

a first metal level disposed over the ferroelectric device level;

an inter-level dielectric level disposed over the first metal level; and

a second metal level disposed over the inter-level dielectric level.

16. The subject matter of claim 15, wherein the contact vias are filled with tungsten contact plugs.

17. The subject matter of claim 16, wherein the ferroelectric capacitors are formed over respective tungsten contact plugs.

18. A method of forming an integrated circuit, comprising:

forming a transistor level comprising one or more semiconductor devices disposed over a substrate and an overlying transistor isolation layer having one or more contact vias extending therethrough;

forming a ferroelectric device level comprising one or more ferroelectric capacitors disposed over the transistor isolation layer and an overlying ferroelectric

isolation layer having one or more vias extending therethrough and laterally sized larger than corresponding contact vias aligned therewith;

forming a first metal level over the ferroelectric device level;

forming an inter-level dielectric level over the first metal level; and

forming a second metal level over the inter-level dielectric level.

19. The subject matter of claim 18, wherein the contact vias are filled with tungsten contact plugs.

20. The subject matter of claim 19, wherein the ferroelectric capacitors are formed over respective tungsten contact plugs.

21. A method of forming an integrated circuit, comprising:

forming a transistor level comprising one or more semiconductor devices disposed over a substrate and an overlying transistor isolation layer having one or more contact vias extending therethrough;

forming an integrated first metal and ferroelectric device level comprising one or more first metal contacts and one or more ferroelectric capacitors disposed over the transistor isolation layer and a ferroelectric isolation layer having one or more vias extending therethrough;

forming an inter-level dielectric level over the integrated first metal and ferroelectric device level; and

forming a second metal level over the inter-level dielectric level.

22. The subject matter of claim 21, wherein the contact vias are filled with tungsten contact plugs.

23. The subject matter of claim 22, wherein the ferroelectric capacitors are formed over respective tungsten contact plugs.

24. The subject matter of claim 21, wherein the integrated first metal and ferroelectric device level has a thickness corresponding substantially to the ferroelectric capacitor heights.

25. The subject matter of claim 21, wherein the integrated first metal and ferroelectric device level is substantially non-planar with a reduced thickness in non-capacitor regions.

26. A method of forming an integrated circuit, comprising:

forming a transistor level comprising one or more semiconductor devices disposed over a substrate and an overlying transistor isolation layer having one or more contact vias extending therethrough;

forming a first metal level over the transistor isolation layer;

forming a ferroelectric device level comprising one or more ferroelectric capacitors disposed over the first metal level and an overlying ferroelectric isolation layer having one or more vias extending therethrough;

forming an inter-level dielectric level over the ferroelectric device level; and

forming a second metal level over the inter-level dielectric level.

27. The subject matter of claim 26, wherein the contact vias are filled with tungsten contact plugs.

28. The subject matter of claim 27, wherein the ferroelectric capacitors are formed over respective tungsten contact plugs.

29. A method of forming an integrated circuit, comprising:

forming a transistor level comprising one or more semiconductor devices disposed over a substrate and an overlying transistor isolation layer having one or more contact vias extending therethrough;

forming a first metal level over the transistor isolation layer;

forming an inter-level dielectric level over the first metal level;

forming a ferroelectric device level comprising one or more ferroelectric capacitors disposed over the inter-level dielectric level and an overlying ferroelectric isolation layer having one or more vias extending therethrough; and

forming a second metal level over the ferroelectric isolation layer.

30. The subject matter of claim 29, wherein the contact vias are filled with tungsten contact plugs.

31. The subject matter of claim 30, wherein the ferroelectric capacitors are formed over respective tungsten contact plugs.

32. A method of forming an integrated circuit, comprising:

forming a transistor level comprising one or more semiconductor devices disposed over a substrate and an overlying transistor isolation layer having one or more contact vias extending therethrough;

forming a ferroelectric device level comprising one or more ferroelectric capacitors disposed over the transistor isolation layer and an overlying ferroelectric isolation layer having one or more vias extending through the ferroelectric isolation layer and the transistor isolation layer;

forming a first metal level over the ferroelectric device level;

forming an inter-level dielectric level over the first metal level; and

forming a second metal level over the inter-level dielectric level.

33. The subject matter of claim 32, wherein the contact vias are filled with tungsten contact plugs.

34. The subject matter of claim 33, wherein the ferroelectric capacitors are formed over respective tungsten contact plugs.